REMARKS/ARGUMENTS

Reconsideration of this application is respectfully requested in view of the foregoing amendments and discussion presented herein.

1. Rejection of Claims 17, 21-22, 25-26, 55, 63-68, 71, 78-80, and 82-85 under 35 U.S.C. §112.

The support for the rejection of these claims indicates only that "*the specification for these claims as first filed does not disclose the following claim limitations*". The rejection has not provided specific information as to what aspect is considered unsupported. Applicant will attempt to make a best-guess as to what is the problem in these claims and to provide information and/or make appropriate amendment.

In addition, Applicant is dismayed that a number of these claims, which contain elements for which not even similar wording is found in the cited references, have not been materially examined, but only rejected on the basis of 112, for example claims 22, 63, 64, 65, 66, 67, 71, 79, 80, 82, 83, 84 and 85.

Claims 17 and 54. These dependent claims recite: "*wherein said input comprises a single signal line coupled directly to each said display element within a given display array, or a signal superimposed on the power being supplied to each said display element within said given display array.*"

The use of a single signal line is supported within embodiments throughout the application and claims, such as with regard to the *Array Position Addressing* (APA) signal which contains both addressing and data for controlling each display element within the array of display elements, and the contents of the optical elements within each of these display elements. The text and drawings clearly show the use of the APA signal and superposition of this signal between power and ground (i.e., FIGs. 2, 4, and 5), and also in the original claims (see Claims 1-4 and 6).

By way of example referring to page 6, line 11 to page 7, line 2: "*The USLEDs of the present invention incorporate what is being referred to herein as Array Position Addressing (APA) which allows the elements to be controllable addressed without the need of individual row and column lines. One aspect of APA on USLEDs involves a technique of in-situ optical programming wherein the USLEDs are programmed from an optical source array (generally a matching, or a*

superset, of the target USLED array) which programs a position address into each USLED on the target array. After programming, each display element retains, such as in FLASH memory, the address within the array that it is to be responsive to. A display array which is implemented according to the present invention contains a collection of programmable display elements, such as USLEDs, which are attached to a surface or backplane containing a power plane and a ground plane. During operation of the display, a drive voltage is applied between the power and ground plane that contains a superimposed serial APA control signal. The APA control signal comprises cycles within which, one or more data bits are contained for each element."

Claim 21. Support for utilizing an input separate from the ground and power plane is found in the specification, such as at page 7, lines 18-22.

Claim 22. Support for Claim 22 is found in FIG. 2, 4, 5, 8 and 9 as well as throughout the specification, including that described above (page 6, line 11 to page 7, line 2).

Claims 25-26. Support for the modulation of the optical state from said latch circuit is described throughout the specification, such as at page 7, lines 4-9; page 8, lines 12-14; and clearly showing the latch FIG. 2 (24) and FIG. 4 (84) driving different optical elements (LEDs) with different colors, including description on page 9, lines 5-17, and so forth.

Claim 55. Support for dependent Claim 55 describing the modulating of the optical state at a fixed position within cycles of the data signal are found throughout the specification, including: page 8, lines 12-14; page 19, lines 11-13; page 20, line 18 through page 21, line 6; page 21, lines 13-18; and so forth. In particular, embodiments describe the reset signal at the fixed position within cycles, for instance being at the end of the cycles, and otherwise describes it as arising elsewhere for random addressing.

Claims 63-68, 71, and 79-85.

It should be noted with regard to Claim 63-68, 71, and 79-85 that the cited references provide no similar structures and not even any similar wording for the programming structures, optical detectors, and integration described in these claims. This is not surprising in that the objects and operating principles of the relied upon references are distinct from that claimed for the instant application. Specifically, there is no means for programming the position address within the elements, as mentioned because they are not directed for use within an array but instead contain and drive an array conventionally. In addition, there is nothing of optical programming in these references. And integration would also not make sense as the relied upon references describe an

entire display which contains a row and column array and a driver circuit for coupling with separate outputs for driving printer row LEDs.

Support for the programming signal is provided in the original claims (Claim 7 is entirely directed to programming of the array address) as well as in the specification, including: page 6, lines 13-18: "*One aspect of APA on USLEDs involves a technique of in-situ optical programming wherein the USLEDs are programmed from an optical source array (generally a matching, or a superset, of the target USLED array) which programs a position address into each USLED on the target array. After programming, each display element retains, such as in FLASH memory, the address within the array that it is to be responsive to.*" This is reflected throughout the specification. It should also be noted that FIG. 5 provides a representation for an embodiment of the programming array in response to the note describing the programming array on page 6, lines 15-16 as "*generally a matching, or a superset, of the target USLED array*", wherein it can have the same structure.

Support for the use of an optical detector is shown in FIG. 2 and 4 as LED 28c, 88c coupled to a comparator circuit 30-32, 90-92 respectively, as the LED is used in both an output mode and as an optical input mode. In addition the optical detector aspect is recited throughout the specification, including page 10, lines 2-13, and so forth.

Support for the use of analog and digital intensity control are also found in the specification, such as at: page 7, lines 1-5; and page 8, line 22 through page 9, line 2.

Support for output control as scanned or random is found through the specification, including: page 10, lines 10-16; page 15, lines 18-20; and so forth.

Support for the incorporating the claimed circuit elements within the die of an optical element, integrated circuit die to which one or more optical elements are bonded is described in the specification, including page 12, line 21 through page 13, line 15.

Therefore, support is provided in the specification for each of the above claims, wherein Applicant respectfully requests that the rejection of these claims be withdrawn.

2. Rejection of Claims 47 and 70 under 35 U.S.C. §102(b).

Claims 47 and 70 have been rejected under 35 U.S.C. §102(b) based on U.S. Pat. No. 5,995,070 to Kitada.

After carefully considering the grounds for rejection the Applicant responds as follows.

It should be recognized at the onset that the Kitada is directed to entirely different objects

and operating principles from the apparatus described in the claims of the instant application. It will be shown below that claims describe aspects of the invention which in no way comport to the teachings of Kitada, wherein these rejections suffer from a number of shortcomings.

Claim 47. This is an independent claim directed to a display element having internal control circuitry, which are described in the claim along with the optical element.

First, the rejection indicates that Kitada discloses a "*display element*" having internal control circuitry. However, Kitada describes a "display" not the elements on the display. This is clearly seen in column 1, lines 22-46, which describes a "*conventional LED display apparatus 1*", which is described as being connected to a display source such as a "*personal computer*". There is no discussion whatsoever of incorporating control circuits within the optical elements themselves. In fact in Fig. 1, 7 and 17 a conventional row/column display device 2 is shown with conventional driver circuits 11, 12 and 13.

This is not surprising in that the object of the Kitada reference is to increase the resolution of a conventional display system, for example as described in the first paragraph of the invention summary as "*to provide an LED display apparatus which is capable of generating color images or pictures of high quality notwithstanding of a small number of dots and low resolution of the apparatus.*"

Rejection ignores "Plain Meaning" of Recited Elements

In positing these rejections the "plain meaning" of the elements being compared has not been considered.

MPEP 2111.01 "PLAIN MEANING" REFERS TO THE MEANING GIVEN TO THE TERM BY THOSE OF ORDINARY SKILL IN THE ART

Furthermore, this plain meaning of the terms is further supported by numerous portions of Applicant's specification, which clearly make the case that the elements would not be considered equivalent by one of ordinary skill in the art.

Consider for example text in the summary of the invention at page 5, line 14 through page 6, line 10. Portions of this text include the following statement.

"*method and system for driving and controlling arrays of display elements. The display elements used within the method can incorporate any conventional type of light modulation element (light generative, or reflective), such as LED, incandescent, laser, LCD, electronic paper, electromechanical, etc.*"

Furthermore, it is said in this text that "*Each USLED element appears similar to a conventional LED, yet contains on-board drivers and control circuitry.*"

Still further it is stated that "*A prime advantage of USLEDs is that they may be arranged into arrays without the need of row and column drivers, and furthermore they do not require a complex backplane containing separate row and column lines. The display elements of the present invention may be easily formed into arrays of any form factor, shape, or curvature without additional complexity. Yet even without row and column signal lines, the display elements are individually controlled.*"

One can also refer to the drawings, such as in FIG. 5, wherein the display elements 114a - 114h are shown appearing as modified LED system coupled in an array each receiving the same two signals coupled to the device in parallel.

Applicant's claim also discusses that the display element and other of these display elements are "within an array of display elements" The display of Kitada includes an array of optical elements, but is clearly not a single display element within an array of other display elements, as required to anticipate the claim.

Kitada teachings NOT Equivalent

It is well settled that for anticipation under 35 USC 102, the anticipating reference must show all the elements of the claim. The above sections began showing that the relied upon reference is not equivalent to the Applicant claim. This shortcoming of the rejection is now fully developed as we discuss the structures described in the claim.

Rejection equates "*a memory configured for programming to a first address associated with the position of said display elements within an array of said display elements*" as being equivalent to fig. 7 (4) of Kitada and the text at column 9, lines 31-47 of that reference.

However, the Kitada reference is being misapplied, as "*display data storage unit*" is configured for a different purpose and IS NOT configured for "*programming to a first address associated with a position of said display element*" to which the claim was drawn towards.

The first problem is that the circuit of Fig. 7 is an entire display and not an element within a display array; wherein there is no position information that needs to be programmed for the element. Column 1, lines 35-36 describe the use of the "*display data storage unit*" as being "*...the display data a stored in the display data storage unit 4 are read out by a display data read out unit*". Accordingly, memory 4 of Kitada contains display data. In addition, there is no discussion of

"*programming*" this memory to a first address - this would have no meaning in the context of Kitada in which memory 4 retains color and intensity information data. By contrast the instant application provides references throughout for the meaning of "programming" this address, such as referring to page 6, lines 15-20, which includes: "*...which programs a position address into each USLED on the target array.*"

Referring to the relied-upon section of Kitada, specifically column 9, lines 31-47, a discussion of how Kitada provides the high resolution as shown in FIG. 2A mapped through four quadrants as shown in FIG. 2B, onto the lower resolution display as shown in FIG. 3A, 3B, 3C and 3D which is output in four stages. A more clear discussion of these aspects is found in column 3, lines 9 - 45, which refers to "*The display in this case is realized by deviating each data group by one LED (i.e., by a half dot.*"

The above teaching of Kitada clearly has nothing to do with the elimination of the need for row and column drivers as provided by the instant application, such as discussed on page 6, lines 11-13: "*The USLEDs of the present invention incorporate what is being referred to herein as Array Position Addressing (APA) which allows the elements to be controllable addressed without the need of individual row and column lines.*" This unit addressability aspects is also discussed throughout Applicant's specification. The elimination of row column addressing is nowhere discussed by Kitada as his system is directed at increasing the resolution of a conventional display 2 driven by conventional row and column driver circuits 11, 12, 13.

As Kitada only discusses the use of a substantially conventional display system with drivers that are separate from the display elements, there is no meaning to the data signals being received in parallel by the cited display element and other display elements in an array of display elements, as Kitada has but one unit.

In support of "*in response to matching a second address received on said data signal with said first address*" the rejection again refers to fig. 7(4) and col. 9, lines 31-47; which was discussed above, and is not relevant. In addition col. 12, lines 46-65 are referred to in support of the rejection. However, this section of Kitada discusses intensity control using counter 8 and comparison unit 9. At the beginning of the discussion of that embodiment of Kitada (refer to column 11, lines 50-65) the overall purpose is disclosed as: "*The second embodiment of the present invention is directed to an LED display apparatus for displaying the data of 16x16 dot matrix on the 8x8 dot matrix type LED display device 2...*", and goes on to discuss aspects of the image data reduction.

However, the above portions of Kitada do not discuss comparing a static position address programmed into the memory with a position address and in response to which the output of at least optical element is modulated from the extracted data. It should be noted that Kitada discusses no extraction of data from "*display data a*" based on position, it brings in a conventional display signal. For enhancing the resolution Kitada selects addresses within memory 4 to then control the overlays, as shown in fig. 3A - 3D. This extraction of data from the display memory is also clearly described in relation to embodiment 3 of Kitada shown by Fig. 9 and 11, and discussed starting at column 13, line 13, wherein an image of a boat and a car can be displayed separately or overlayed on one another, yet the data is both contained in display memory. Therefore it is quite clear that the teachings of Kitada do not comport to these elements of Applicant claims.

To support an anticipation rejection, every claim element must be taught or inherent in a single prior art reference, Manual of Patent Examining Procedure (MPEP) §706.02a. The claims elements recited within independent Claim 47 do not comport to the teachings of Kitada, therein the amended claims are not anticipated therefore by the relied-upon reference.

Therefore, Applicant respectfully requests that the rejection of Claim 47 and the claims which depend therefrom, be withdrawn and the patent allowed to issue.

Claim 70. Claim 70 is an independent claim directed to a display element having internal control circuitry, which is described in the claim along with the optical element. The rejection of Claim 70 suffers from similar shortcomings as those described with regard to Claim 47 above. It will be noted that similar storage of a display unit position address is described and that data, received in common by all display elements within a display array, is output in response to matching the position in the array with an address in the data, at which time optical state data is taken from the data signal for controlling the state of the optical elements in the display element.

Although Claim 70 already overcomes the cited reference, Applicant has amended the claim into a form which it is hoped will more clearly point out the operation of the device. In particular Claim 70 now describes in more detail the about the first memory, which stores a position address value in response to programming, and which retains this first address during operation of the display element. The nested elements were pulled out into additional means terms, specifically "means for receiving" and "means for matching", more clearly in line with their importance.

Therefore, Applicant puts forth that independent Claim 70 is no anticipated by the relied-upon reference and furthermore that the claim amendments even further distinguish from the

reference. Applicant respectfully requests that the rejection of Claim 70, and the claims that depend therefrom, be withdrawn.

3. Rejection of Claims 16 and 61 under 35 U.S.C. §103(a).

Independent Claims 16 and 61 were rejected under 35 U.S.C. § 103(a), as being obvious over U.S. Pat. No. 5,995,070 to Kitada in view of U.S. Pat. No. 5,233,337 to Takahashi.

Numerous shortcomings of this rejection, based on the primary Kitada reference are addressed herein, as the elements of the claim have been incorrectly equated to aspects of that reference although the teachings therein are clearly drawn to different objects and operating aspects than the instant application.

A mistake made throughout these rejections is that of dissecting Applicant's invention into a number of words and phrases and finding the same or similar words in a reference and positing a rejection. However, proper support for a rejection requires that the same structures of an apparatus, or steps of a method, be taught in the subject claims as in the recited references. Therein one must go beyond a simple word search and compare the teachings as a whole, taking into account what those word and phrases mean in each instance as well as how those elements interact with one another.

Different Objects and Operating Principles

As discussed in relation to Claims 47 and 70, above, the Kitada reference is directed to increasing the resolution of an otherwise conventional color display, by using a system of overlaying pixel data on one another. It does not disclose a "*display element*" "*having internal optical output control circuitry*" for incorporation within an array of display elements. The system of Kitada does not teach incorporating the described circuitry within each display element (i.e., pixel) of a display array. Clearly the object of the system of Kitada is not directed at eliminating the need for row and column drivers, as these are used conventionally as seen in FIG. 1 and FIG. 7, nor can it provide the benefits which are brought out in the specification of the instant application.

Elements In References Are Not Equivalent

In support of the rejection numerous claim elements are improperly equated to elements within the Kitada reference, as was similarly pointed out with regard to claims 47 and 70 in a prior section.

As brought out above Kitada does not describe a display element, which is configured for being but one in an array of such elements, but instead an entire display in itself.

Support for "*an input configured for receiving an array position addressing signal containing array position clocking and data which are delivered in common to all said display elements within a single or multidimensional display array*" is improperly equated to col. 12, lines 25-27 of Kitada with no explanations given.

However, that section merely states: "*The display data a supplied from the display signal generation source is received by the display data receiver 2 under the timing giving by the synchronizing signal b*". It is quite clear that this describes clocking of data into the display memory of the Kitada device, there is nothing which describes delivering the data to be used by a plurality of different display elements. Applicant claim describes a single display element which receives the same signal as an array of elements. It receives a "position addressing signal" based on its position in that array. These aspects are not taught, not inherent, within the Kitada reference.

The rejection then again dissects elements and attempts to compare them with similar words used in Kitada, again without properly discerning the meanings therein. Specifically, the rejection only points out memory 4 in fig. 7 and makes an assertion that this is for holding array position, however, this is not put forth within Kitada because it discloses a single display that contains its own array of elements, which is entirely different. Memory 4 is just a conventional display memory (col. 1, lines 35-36) "...the display data a stored in the display data storage unit 4 are read out by a display data read-out unit". There is no teaching of this being for storage OR comparison of array position in the Kitada reference.

The claim element "*a counter configured for maintaining an array position count in response to detecting said array position clocking from said input*" and "*a comparison circuit configured for generating a data load signal in response to detecting a desired relationship between said array position maintained by said counter and said array position retained in said memory*" is improperly compared to elements 11-13 in Kitada (no additional explanation is provided).

However, the counter of Kitada has nothing to do with determining if the data is directed to this display element as one display element in an array of such display elements, but instead establishes the length of time that an element is active, referring to col. 1, lines 57-67, is included the statement: "*In that case, so long as the count value is smaller than "128" inclusive, the comparison unit 9 outputs a light emission enable signal (e.g., H-level signal) for enabling light emission of the LED. On the contrary, when the count value exceeds "128", the comparison unit 9 outputs a light emission inhibit signal (e.g., L-level signal) for disabling or inhibiting the light*

emission of the LED." So this is the conventional practice of converting the intensity information within memory 4 and converting this into an intensity level. There is nothing relating to the position of this display element in relation to other display elements of an array - again this should not be confused with elements that are within an internal array, such as in LED array 2 as shown in Fig. 1 of Kitada. The display element of Applicant claims is an element within an array of these elements and it extracts it own position and data from a signal in common with all the display elements in the array.

Similarly, the comparison circuit of Kitada has no bearing or semblance of "generating a data load signal" in response to position in the array as required by the claim. The comparison unit 9 of Kitada as discussed in the prior paragraph controls the active/inactive state and this intensity of each LED within the multiplexed row and column LEDs in the display.

In support of the combination the teachings of Takahashi are brought in. The reason for this combination belies much of the problem with the entire rejection. The combination is made because "*Kitada has failed to teach a latch circuit*". This underscores the problem with attempting to dissect the instant application and making comparisons on a piecemeal basis with other references. Numerous circuits are built using resistors, transistors, capacitors, inductors, or logic circuits, as these are the building blocks of all electronic circuits, however, the patentability of these inventions has nothing to do with whether these building blocks are used elsewhere. Just as in a chemical patent application, it can only draw from the known elements, but this in no way detracts from its patentability.

The rejection attempts to build the claimed invention from piecemeal electronic elements which of course runs contrary to proper examination practice. The combination must be workable to accomplish the same end, and the motivation to combine must be taught or suggested by the references. The addition of a "latch" still does not provide for extracting data for the display element from the common signal to all display elements in an array of display elements based on display element position within that array. Therefore, the combination is unworkable.

Numerous Additional Shortcomings of Rejection

The rejection suffers from a number of other shortcomings, which will only be touched upon, as the above problems are so intractable.

A lack of specificity of suggestion to modify exists. Combinations must provide specificity on how the modification is made and how it provides the same functions. Combination is

unworkable for a number of reasons, the latch of Takahashi is not even latched by an internal signal, but by external signal 74. And numerous other problems.

Combination is useless. Adding a latch to the comparator of Kitada does not improve its function, actually the data in display data storage is static once loaded anyway and data for intensity for pixels is being read out of it.

Invention must be considered as a whole. The structures and functions of the invention which is brought out in the claims must be considered as a whole, NOT as a collection of circuit elements.

Accordingly, it is clearly seen that the claims elements have been improperly compared to elements of Kitada which provide different functions. Therefore, Applicant respectfully requests that the rejection of Claims 16 and 61, and the claims that depend therefrom, be withdrawn.

4. Rejection of dependent Claims 17-26, 48-60, 62-68, and 71-78 under 35 U.S.C. §103(a).

Dependent Claims 17-26, 48-60, 62-68, and 71-78 were rejected under 35 U.S.C. § 103(a), as being obvious over U.S. Pat. No. 5,995,070 to Kitada in view of U.S. Pat. No. 5,233,337 to Takahashi.

First, in view of the patentability of their respective independent claims, the above claims should be considered *a fortiori* allowable. In addition, the majority of above claims recite elements which in no way comport to the relied upon teachings. A number of these shortcomings are briefly discussed below.

Claims 17 and 54. In attempting to support the rejection fig. 4 and 7 (24, 68) are relied upon of Takahashi, which is said to "*disclose a single signal line*". Again the teachings of the claim have been removed from their textual context of the dependent claim, as well as removed from their context in relation to the base claim from which it depends. These dependent claims describe how data from a single signal line is used by a plurality of separate display elements within a display array, which of course is possible because of the position addressing described. However, this is incorrectly equated to the single signal line shown in Takahashi. Connecting multiple circuits shown by Takahashi to this one signal lines does not result in creating a display array, because the LEDs in each of these circuit would of necessity display the exact same patterns, there is no mechanism for discerning one from another and certainly nothing as disclosed with regard to the storing of a position address and the comparison in response to the data on the common signal.

Therefore, no support exists for the above rejection and Applicant respectfully requests it be withdrawn.

Claim 20. In support of the rejection it is said that the memory is loaded with "*an array position value in response to a position programming operation*", and fig. 7(6), col. 10, lines 19-32 of Kitada are relied upon.

However, neither the figure nor the text of Kitada provides any such teaching. As mentioned in relation the independent claims, "address determining unit 6" of fig. 7 of Kitada is for a completely different purpose. The address determining unit clearly generates addresses so that the data can be read from memory 4 for display on the plurality of LEDs 2. This is actually clearly spelled out by the relied upon section of column 10, lines 19-32, as stated "*...the content of the read-out operation counting unit 7 is incremented while the address determining unit 6 determines the address corresponding to the updated content of the read-out operation counting unit 7...*".

A reading of the instant application should make this position programming aspect clear. The Abstract brings out this important point: "*Each display element is loaded with an address of where it is located within the array. The display elements then extract the display information from the signal upon matching the address, wherein they output the correct display setting for their position within the array.*" For example in the summary on page 6, lines 11-13: "*The USLEDs of the present invention incorporate what is being referred to herein as Array Position Addressing (APA) which allows the elements to be controllable addressed without the need of individual row and column lines.*" By way of example the position programming of a display element is described on page 10, lines 16-18: "*It will be appreciated that should the arrays be optically-coupled face to face, then the preprogrammed USLED array should be programmed as a mirror-image of the addressing for the array being programmed.*" The addressing being spoken of is array position addressing. Each display element is programmed with a position value in the array; the position value determines what data is extracted from the common data line.

Accordingly, as Kitada does not teach this aspect it does not suppoit the rejection, wherein the rejection should be withdrawn.

Claim 22. The material rejections do not include independent Claim 22 directed at the data being superimposed over the power and ground (though a 112 rejection is put forth) as neither of the references provide this aspect, nor would benefit from its as they are directed to different objects and operating principles.

Claim 23. In support of "*wherein said array position clocking and data are received for each array address in each cycle of an array position addressing signal*" the rejection only indicates "see fig. 7 (10,12)". However, the light emission driver control circuit 10 and light emission driver circuit 12 have no relation with array position clocking as recited in the claim. Kitada shows conventional driving of LEDs within a display wherein data for the whole array is stored in memory 4, then clocked out and passed through row and column drivers to an array of LEDs. The instant application describes that each element of the display array has circuitry wherein it extracts its own data from the signal based on array position addressing. There is nothing within either reference that bears on "*array position addressing*" as taught within the instant application.

Claims 48-49. Dependent claims 48 and 49 refer to the array position address stored in memory which establishes the position of the display element in the array. This is improperly compared to the LEDs in the array having one or more axis. Neither reference provides any teachings which comports to array position addressing. The display of Kitada is an entire display not one display element in an array, and similarly Takahashi teaches a unit which controls a linear array by itself. There is no position addressing of the display element in either cited reference. The instant application provides for addressing of the unit itself to replace the needs of physical row/column addressing and on a lower level to drive the actual pixels with data provided. The cited references provide a substantially conventional means of driving an array of dumb elements (without internal control circuits), and thus do not equate to the claims of the instant application.

Claim 51. Dependent Claim 51 refers to a mechanism for getting the data for driving this particular display element within an array of display elements. This mechanism is based on "*array position addressing*" as discussed previously which is not taught by the references. Specifically, the claim recites: "*wherein said means for extracting data is configured for counting clocks on said data signal for determining said second address.*" The first address is array position address to the display element (the whole circuit with optical elements) is programmed too, and the second address is being generated in response to clocks coming off of the shared signal. When the clock counts to a value that matches then the data is pulled off the signal for the optical elements contained on this specific display element. There is no support for these aspects in the relied-upon reference.

Consequently, the rejection of the dependent claims should be withdrawn.

5. Patentability of Independent Claims 69, and 85-87.

Claim 69. No grounds for rejection were given in support of the rejection of independent Claim 69.

The claim is directed to an integrated display element having an optical element and circuitry. The position of the display element within an array of these display elements is stored in a first address and data is extracted from a common data signal, received in parallel by other display elements, in response to matching first and second addresses. As discussed in relation to Claims 16 and 61, support is lacking in the relied-upon references.

Claims 85, 86 and 87. Independent claims 85-87 each describe the display elements of the invention and include the limitation of an optical detector configured for the programming the position address within the display element.

These additional aspects are not discussed with regard to the cited references and they are clearly patentable over the cited references.

Therefore Applicant respectfully requests the rejection of the above claims and the claims which depend therefrom be withdrawn.

6. Amendment of Claims 70 and 85-86.

Claim 70. Independent Claim 70 has been amended to recite aspects of the invention with greater clarity. It now incorporates elements from both claims 47 and 85.

Claim 85. Independent Claim 85 has been amended to increase clarity. In particular the recitations on the different possible makeup of the optical detector are removed.

In addition, the display element is characterized as being responsive to the programming signal for loading said second address, and not by other display elements within [[an]] a same array of display elements which are not ~~to respond~~ responsive to said second address. This should increase the clarity with regard to programming of the position address value into the display element.

Claim 86. Independent Claim 86 has been amended to include information about the memory which is configured for retaining the position address; in that it retains this information during operation and until the memory is reprogrammed to a different address. Thus the memory is not a pixel buffer which is constantly being overwritten with new data as the output of displayed pixels changes. Support is found throughout the specification including: page 6, lines 17-18; page 10, line 20 through page 11, line 12; page 17, line 21 through page 18, line 1; page 18, lines 16-19;

page 22, line 19 through page 24, line 16; and so forth.

In addition amended claim 86 describes how the display element is controllable addressed within an array of those display elements, without the need of using row and column lines coupled to the display elements. This aspect is a basis premise of the present invention as it overcomes a number of shortcomings of driving conventional displays, wherein support for this is abundantly found throughout the specification, for example page 6, lines 2-13; page 11, line 19 through page 12, line 1; page 13, lines 9-12; page 14, lines 15-17; page 15, lines 15-17; page 30 lines 13-16, and so forth.

7. Addition of Claims 88 - 107.

Claims 88, 91, 94, 97, 100 and 103. These dependent claims recite aspects of the memory for retaining the array position in greater detail. In particular that the memory retains the array position during both operation and power down and until it is reprogrammed to a different address. It is seen that embodiments describe programming (not simply writing) the position address in both non-volatile or one-time programmable memory which then retains the address during the described operations, and the address only being set through a distinct programming sequence as described throughout the text. Support is found throughout the application, including FIG. 2 - 4, original claims 3 and 7, as well as in the text of the specification, such as: page 6, lines 17-18; page 11, lines 4-12; page 12, lines 2-4; page 12, lines 11-13; page 17, line 21 through page 18, line 1; page 18, lines 16-17; page 23, lines 3-8; page 24, lines 3-8; page 24, lines 15-16; and so forth.

Claims 89, 92, 95, 98, 101 and 104. These dependent claims recite how the display element is configured for electrical connection to a base member having parallel conductive planes through which power as well as a data signal are communicating to each display element within a plurality of the display elements. This brings out a key aspect of the invention which allows creating simple display arrays wherein the only backplane necessary comprises conductive sheets (i.e., 2 or 3) separated by an insulator. This aspect is shown in schematic in FIG. 5-6 and with the sheets in FIG. 7-8. In addition, a two conductive sheet backplane is found in original Claim 8 as the "array support member". Support is also found throughout the text, including: page 5, lines 7-9; page 6, lines 4-10; page 14, lines 15-17; page 29, lines 8-17; page 30, lines 5-16; and so forth.

Claims 90, 93, 96, 99, 102 and 105. These dependent claims recite how the display elements operate in an array without the need of individual row and column signal lines. Support is found throughout the text, such as in the same references listed above.

Claim 106. Independent Claim 106 is substantially a combination of pending Claims 47 and 85 with some phrasing changes. The optical element, memory and means for modulating are used from Claim 47 with certain programming aspects of Claim 85. The circuitry described in this claim is part of an integrated circuit as described throughout the specification, including: page 12, line 21 through page 13, line 9; page 13, line 18 through page 14, line 4; page 17, lines 15-16; and so forth.

Claim 107. Claim 107 depends from independent Claim 106 and recites the superposition of the data signal on power being supplied to the display elements. This is brought out in prior claims and throughout specification.

Claim 108. Claim 108 depends from independent Claim 106 and recites the use of a separate data signal supplied in parallel with other display elements. This is brought out in prior claims and throughout specification.

Claim 109. Independent Claim 109 is based on Claim 16, but leaves out some elements of clocking specific to that particular embodiment. Claim 107 includes description of the display element being configured for operation within an array of display elements coupled to a base member having parallel conductors which bring power and data, in parallel, to all display elements within the display array.

Claim 110. Claim 110 depends from independent Claim 109 and recites that the display element provides an electrical pinout of two or three contacts adapted for connection to a base member to which an array of the display elements can be attached. This aspect cover the case of the data superposed on the power or a separate data line, within the parallel conductors connecting each of the display elements. Support is found throughout the specification, including: page 6, lines 3-7; page 7, lines 18-22; and so forth.

None of the amendments have been made for the purpose of overcoming any ground for rejection or addressing any cited reference. Nor do any of the amendments made narrow the scope of the claims.

8. No Additional Claim fees are due.

No additional claim fees are required for adding claims 86-107, because claim cancellations executed in addressing previous restriction requirements in the case, has reduced the number of pending claims sufficiently below the number of claims for which a payment has been made.

Prior fees covered a total of 72 claims including 10 independent claims. The added claims

bring the total claims back up to 72 including 10 independent claims.

Accordingly, the number of independent claims and total claims within the instant application do not exceed the number which have been paid for in the application.

9. Extension of Time Petition.

The Applicant has enclosed a petition for a one three-month extension of time to respond to the Office Action and has enclosed the appropriate petition fee.

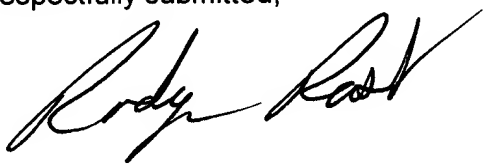
10. Conclusion.

Each of these presently pending claims in this application are believed to be in immediate condition for allowance.

The Applicant respectfully requests a response/interview (email/phone) with the Examiner to clarify any issues that arise upon examination on the merits of the present application, if an allowance of all claims does not appear forthcoming.

Date: Sept. 15, 2006

Respectfully submitted,



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